High-Performance and High-Yield Ka-Band Low-Noise MMIC Using 0.25-μm Ion-Implanted MESFET's

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Abstract—**Three-stage low-noise amplifiers fabricated using high-yield 0.25-μm ion-implanted process showed 4.2 dB average noise figure with a 15-dB gain in Ka-band.**

I. Introduction

TO minimize the cost of MMIC's, it is important to achieve the highest yield possible without sacrificing performance. This is especially true where the MMIC's are required in very high volume (e.g., smart ammunitions, phased arrays) without making the system cost prohibitive. Ion-implantation technology is a viable option for fabricating MMIC's at low cost. The aim of this work was to maximize the performance of this relatively cheap MMIC technology to cater to high-volume needs.

Hybrid low-noise amplifiers (LNA's) using discrete ion-implanted devices on heterostructure substrate [1] have produced impressive results in Q-band. The same group reported [2] Q-band MMIC-amplifier performance using ion-implanted technology with no noise data. In this letter, we present the performance of LNA MMIC in Ka-band using only ion-implantation technology.

II. Fabrication

The LNA IC's are based on 0.25 μm ion-implanted FET technology fabricated on a 3-inch wafer using a hybrid e-beam/stepper lithography process. All lithography except the 0.25-μm gate level is done with a Censor 10x optical stepper. The gate lithography uses e-beam direct-write exposure. The IC's use dual-channel implants of Si^{29} $1e1$ cm^{-2} at 100 keV and 50 keV with a buried p implant of Be $6e11$ cm^{-2} at 80 keV to improve transconductance of the FET's when they are biased near pinchoff. Backside processing includes thinning the wafers to 4 mils, reactive ion etching of via holes, gold plating the backside, and etching the streets for chip separation.

III. Design and Results

The design approach utilizes three 0.25 $\times$ 100-μm^2 MESFET's (each having four fingers 25-μm wide) for the three stages of the amplifier. The dc characteristics (V_{DS} = 2V) of these FET's are shown in Fig. 1. Three device characteristics from three stages are superimposed together. These three devices were measured from one of the amplifier samples measured. Each stage of the amplifier uses series source feedback to improve the input reflection while bringing the optimum noise impedance closer to the input match. The gate bias has stabilizing resistors. The drain bias is fed over RF-shorted quarter-wave lines that are connected at the lowest impedance points in the drain circuit of the devices. This biasing arrangement makes the amplifier unconditionally stable up to f_{max} of the device. Fig. 2(a) shows the chip layout for the amplifier; it measures 1.08 $\times$ 2.53 mm^2. Fig. 2(b) shows the circuit schematic for the amplifier. The microstrip discontinuities are modeled using the software LIBRA-2.1 Fig. 3 shows the equivalent circuit model and noise parameters of the device (0.25 $\times$ 100 μm^2) at low-noise bias point (V_{DS} = 2V, I_{DS} = 20% I_{DSS}). Fig. 4 shows the measured gain and input reflection of five amplifiers superimposed together. Fig. 5 shows the measured output reflection of the same five amplifiers. These five amplifiers were taken from the same wafer, from different reticle locations (one at the center of the wafer and the other four approximately at four corners). Fig. 6 shows the measured noise figure of two amplifiers at low-noise bias points (20%-25%-35% I_{DSS} @ V_{DS} = 2V). The plot is shown on an expanded scale. The noise figure is well below 5 dB over most of 30–36 GHz; it has an average noise figure of 4.2 over the band 30–36 GHz. Because of input and output reflection, the usable bandwidth is 31–35 GHz. The noise figure goes down to 3.8 dB at 34 GHz with 16 dB of gain. The results presented here for a multistage Ka-band low-noise MMIC with very low cost ion-implantation technology are the best according to the authors' knowledge.

The RF yield of the circuit was determined by setting a window on the small signal gain G, for example $G \pm 1.5$ dB. The value of G differs from wafer to wafer, but its minimum and maximum limits are set by the system requirement (e.g., $10 \leq G \leq 15$). With this definition, the RF yield showed as high as 70% on the best wafer. The results reported here are from this best wafer. The yield data are being incorporated in [3].

IV. Conclusion

We have demonstrated a high-performance Ka-band LNA MMIC using high-yield ion-implantation process. The RF yield based on small signal gain reached a reasonable value

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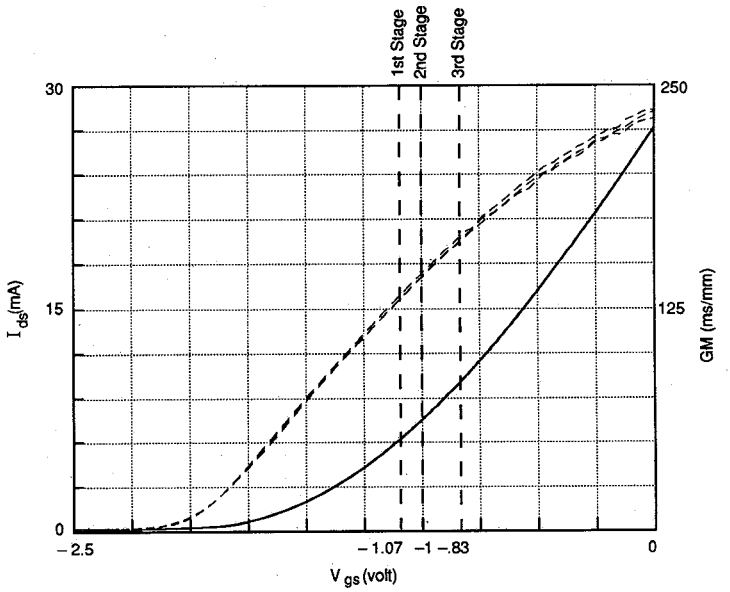


Fig. 1. dc characteristics of 0.25 × 100-μm^2 ion-implanted FET used in the design. Also shown are the bias points where the stages were biased for RF performance V_{DS} = 2V.

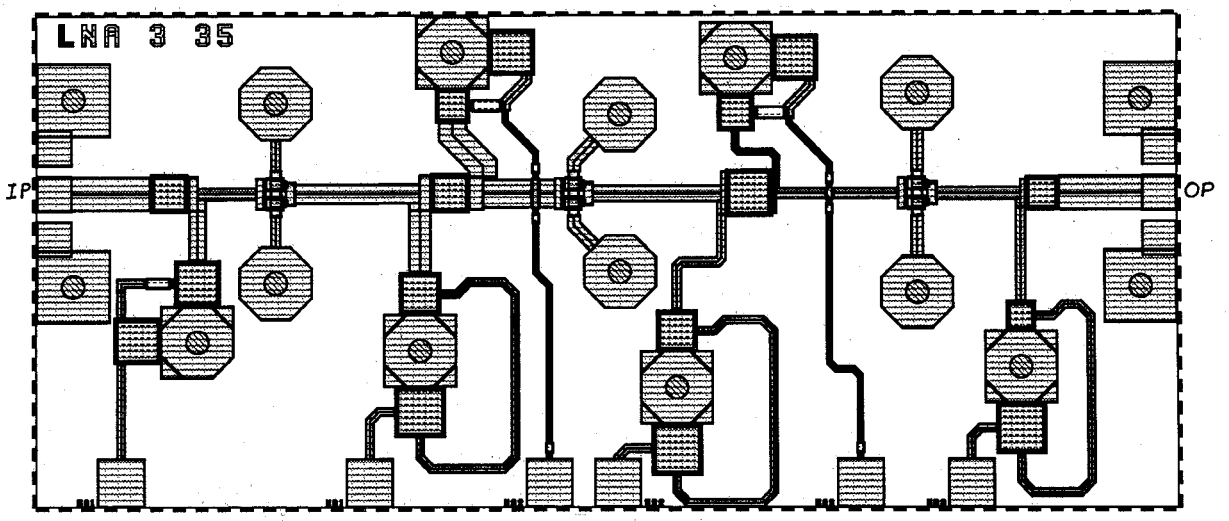


Fig. 2(a). Chip layout for the three-stage LNA MMIC (1.08 × 2.53 mm^2).

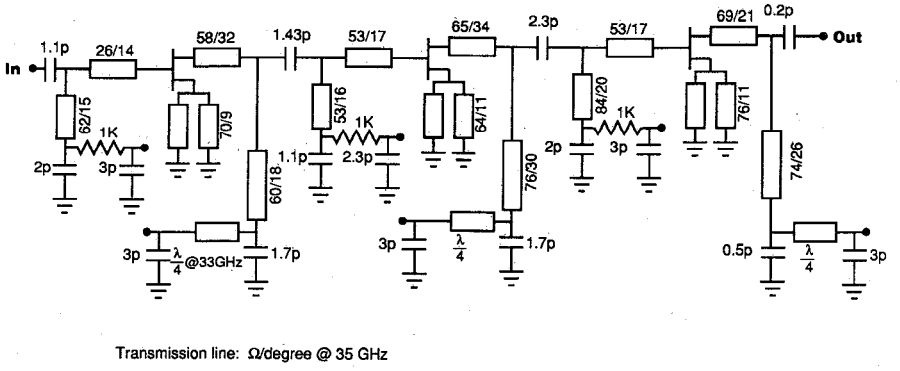
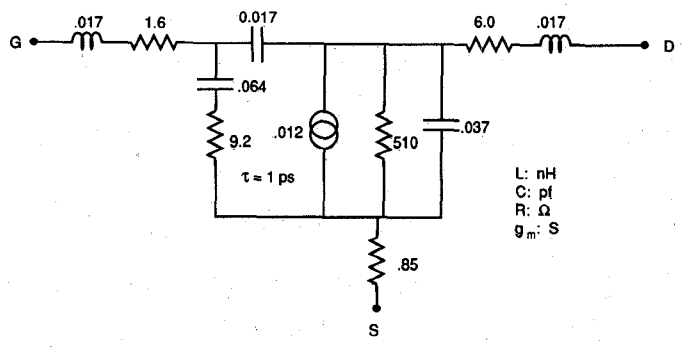


Fig. 2(b). Circuit schematic for the three-stage amplifier.



Freq. (GHz)	F_{min} (dB)	Γ_{opt}	r_n
30	3.0	0.75 ∠ 74°	1.9
33	3.2	0.73 ∠ 79°	1.8
36	3.4	0.72∠ 85°	1.72

Fig. 3. Equivalent circuit and noise parameters of the device at low-noise bias point (V_{DS} = 2V, I_{DS} = 20% I_{DSS}).

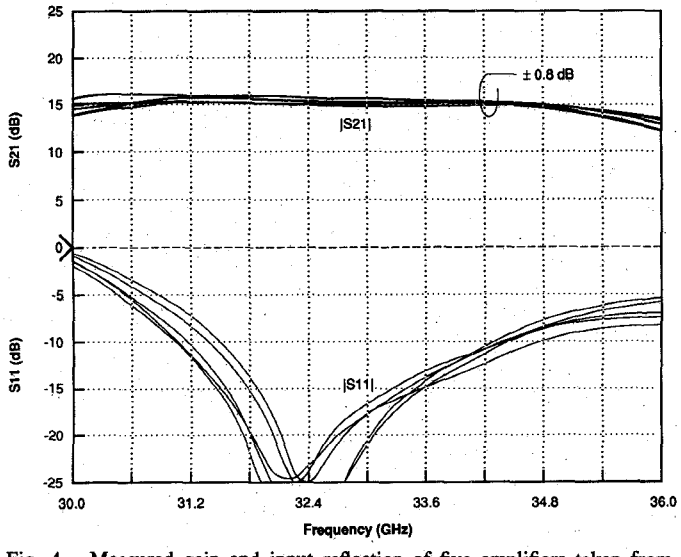


Fig. 4. Measured gain and input reflection of five amplifiers taken from five reticles over the same wafer.

on the best wafer. This relatively inexpensive technology, if maximized for the performance, shows a good promise in applications where unit cost is critical and volume is high.

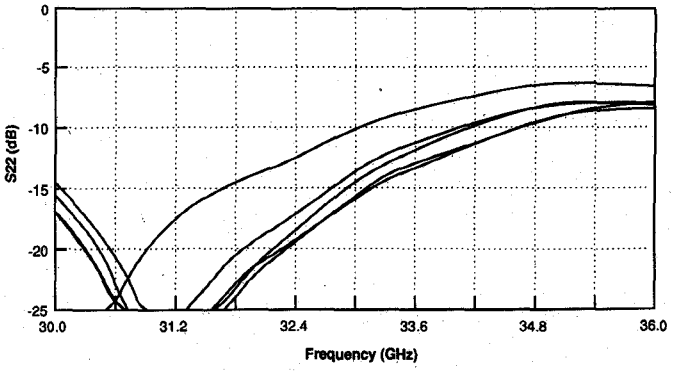


Fig. 5. Measured output reflections of the same five amplifiers.

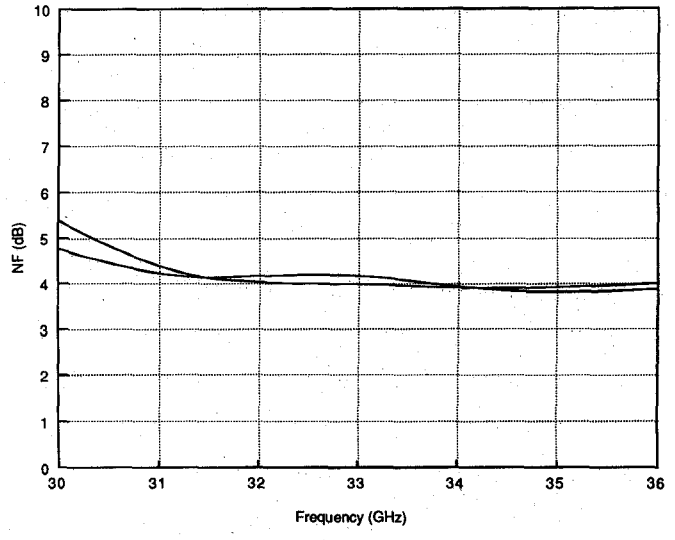


Fig. 6. Measured noise figure of two amplifiers on an expanded scale from 30–36 GHz. The bias voltage remains fixed. V_{DS} = 2V, V_{GS1} = −1.07V (~ 20% I_{DSS}), V_{GS2} = −1.00V (~ 25% I_{DSS}) and V_{GS3} = −0.83 (~ 35% I_{DSS}).

References

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[3] J. Mondal, J. Geddes, D. Carlson, and M. Vickberg, "Yield of Ka-band MMIC's using 0.25-μm MESFET process on MBE and ion-implantation material," submitted to *IEEE Microwave Guided Wave Lett.*